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EXAMINER	
BAKER, STEPHEN M	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,861	LEUNG ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *110806*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,933,436 to Tanzawa *et al* (hereafter "Tanzawa").

Tanzawa discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Tanzawa's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding. Tanzawa states that when no error correction is performed on read data that has a detected error, a signal NOTCOR is activated (column 11, lines 7-12), which is understood to mean that read data that is in error but cannot be corrected is output as is, uncorrected, as no arrangements for otherwise changing the data in error is disclosed.

Tanzawa does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

Official Notice is taken that the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was well known at the time the invention was made, and furthermore, any data written to a memory can be inherently considered a "test data pattern." It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-

supplied "test data pattern" to Tanzawa's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Tanzawa's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the semiconductor memory system disclosed by Tanzawa. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

3. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,177,743 to Shinoda *et al* (hereafter "Shinoda").

Shinoda discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Shinoda's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding.

Shinoda does not suggest changing uncorrectable data.

Official Notice is taken that outputting uncorrected data when the data is uncorrectable is the simplest and easiest way for an ECC decoder to operate. Furthermore it is noted that, absent any special means to modify uncorrectable data, it must be assumed that uncorrectable data remains uncorrected. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Shinoda's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Shinoda does not suggest changing uncorrectable data.

Shinoda does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-supplied "test data pattern" to Shinoda's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory

chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Shinoda's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the semiconductor memory system disclosed by Shinoda. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

4. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinoda in view of U.S. Patent No. 4,939,694 to Eaton *et al* (hereafter "Eaton").

Official Notice is taken that outputting uncorrected data when the data is uncorrectable is conventional in semiconductor storage systems using ECC, as evidenced by Eaton (column 8, lines 55-58). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Shinoda's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Eaton evidences that leaving uncorrectable data unchanged is conventional in semiconductor storage ECC.

5. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,706,248 to Masaki (hereafter "Masaki").

Masaki discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Masaki's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding.

Masaki does not suggest changing uncorrectable data.

Official Notice is taken that outputting uncorrected data when the data is uncorrectable is the simplest and easiest way for an ECC decoder to operate. Furthermore it is noted that, absent any special means to modify uncorrectable data, it must be assumed that uncorrectable data remains uncorrected. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Masaki's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Masaki does not suggest changing uncorrectable data.

Masaki does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-supplied "test data pattern" to Masaki's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Masaki's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the

semiconductor memory system disclosed by Masaki. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

6. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masaki in view of Eaton.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Masaki's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Eaton evidences that leaving uncorrectable data unchanged is conventional in semiconductor storage ECC.

7. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,726,021 to Horiguchi *et al* (hereafter "Horiguchi").

Horiguchi discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Horiguchi's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding.

Horiguchi does not suggest changing uncorrectable data.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Horiguchi's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Horiguchi does not suggest changing uncorrectable data.

Horiguchi does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-supplied "test data pattern" to Horiguchi's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Horiguchi's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the

semiconductor memory system disclosed by Horiguchi. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

8. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi in view of Eaton.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Horiguchi's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Eaton evidences that leaving uncorrectable data unchanged is conventional in semiconductor storage ECC.

9. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,151,906 to Sawada (hereafter "Sawada").

Sawada discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Sawada's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding.

Sawada does not suggest changing uncorrectable data.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Sawada's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Sawada does not suggest changing uncorrectable data.

Sawada does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-supplied "test data pattern" to Sawada's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Sawada's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the

semiconductor memory system disclosed by Sawada. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

10. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada in view of Eaton.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Sawada's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Eaton evidences that leaving uncorrectable data unchanged is conventional in semiconductor storage ECC.

11. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,535,226 to Drake *et al* (hereafter "Drake").

Drake discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Drake's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding.

Drake does not suggest changing uncorrectable data.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Drake's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Drake does not suggest changing uncorrectable data.

Drake does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-supplied "test data pattern" to Drake's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Drake's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the

semiconductor memory system disclosed by Drake. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

12. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drake in view of Eaton.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Drake's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Eaton evidences that leaving uncorrectable data unchanged is conventional in semiconductor storage ECC.

13. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,549,460 to Nozoe *et al* (hereafter "Nozoe").

Nozoe discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Nozoe's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding.

Nozoe does not suggest changing uncorrectable data.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Nozoe's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Nozoe does not suggest changing uncorrectable data.

Nozoe does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-supplied "test data pattern" to Nozoe's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Nozoe's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the

semiconductor memory system disclosed by Nozoe. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

14. Claims 1-6, 8, 9, 11-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozoe in view of Eaton.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Nozoe's semiconductor memory such that uncorrectable data is output unchanged. Such a realization would have been obvious because Eaton evidences that leaving uncorrectable data unchanged is conventional in semiconductor storage ECC.

15. Claims 1-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,052,816 to Yoshinogawa (hereafter "Yoshinogawa").

Yoshinogawa discloses a memory chip with built-in error correction code encoding and decoding, thereby providing a "semiconductor memory having transparent error correction." Yoshinogawa's ECC decoder leaves correct data unchanged and corrects correctable data, in the conventional manner for ECC decoding. Uncorrectable data is purposefully changed by a 'different data generating circuit' (5).

Yoshinogawa does not specifically mention writing an externally-supplied "test data pattern" to the memory chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply an externally-supplied "test data pattern" to

Yoshinogawa's memory chip. Such an application would have been obvious because the reliability-improving usefulness of writing an externally-supplied "test data pattern" to a memory chip was already well known, and any data written to a memory can be inherently considered a "test data pattern."

Regarding claims 3-6, 8, 11, 12 and 14, Official Notice is taken that Hamming codes, comparison of read and recalculated check bit bits in order to generate a syndrome, and also generating single-bit error and multiple-bit error status signals from a syndrome were all conventional in semiconductor memory ECC systems at the time the invention was made. It would have been obvious to implement Yoshinogawa's code, syndrome generation and syndrome decoding in accordance with claims 3-6 8, 11, 12 and 14,. Such an implementation would have been obvious because the limitations of claims 3-6 8, 11, 12 and 14 were already conventional in semiconductor memory ECC systems.

Regarding claims 2, 13, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the semiconductor memory system disclosed by Yoshinogawa. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

Response to Arguments

16. Applicant's arguments with respect to claims 1-17 and 19-23 have been considered but are moot in view of the new grounds of rejection.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb